Serial real time clock IC

Description

The DS1302 is a slow-speed chargeable real-time clock (RTC) chip featuring a real-time clock/calendar and 31 bytes of non-volatile static RAM. It communicates with a microprocessor via a simple serial interface. The real-time clock/calendar counts seconds, minutes, hours, days, weeks, months, and years, automatically adjusting month-end dates for months fewer than 31 days and incorporating leap year correction. The clock operates in either a 24-hour format or a 12-hour format with AM/PM indication. The 31 bytes of RAM can temporarily store important data. Synchronous serial communication simplifies interfacing the DS1302 with a microprocessor, requiring only three wires: (1) RST (reset), (2) I/O (data line), and (3) SCLK (serial clock). Data can be transmitted in single-byte format or multi-byte format up to 31 bytes at a time. The DS1302 operates at very low power consumption, preserving data and clock information with less than 1μW of power.

Features

- Counts seconds, minutes, hours, days, weeks, months, and leap year-compensated years.
- Features 31 bytes of non-volatile static RAM for high-speed data storage.
- Wide operating voltage range: 2.0V to 5.5V.
- Low power consumption of less than 300nA at 2.5V.
- Supports single-byte or multi-byte data transfer for clock or RAM data read/write operations.
- Simple 3-wire interface for communication with microcontrollers.
- TTL compatible (V_{CC}=5V).
- Optional industrial temperature range from -40°C to +85°C.
- Package options: DIP8 and SOP8.

Applications

- Prepayment electric meters, IC card water meters, IC card gas meters
- Fax machines
- Portable instruments
- Mobile phones

Product information

Product Name	Package	Print Name	Package
DS1302	DIP-8	DS1302	tube
DS1302Z	SOP-8	DS1302Z	taping
DS1302N *	DIP-8	DS1302N	tube
DS1302ZN *	SOP-8	DS1302N	taping

* The ones with N are industrial grade

Block diagram and pin functions

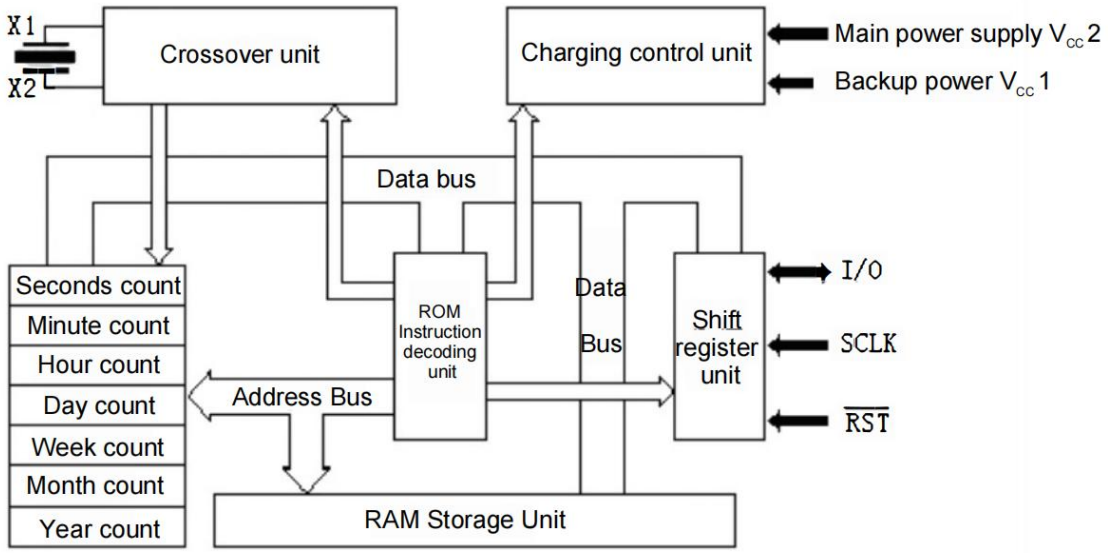


Fig.1 DS1302 Internal Block Diagram

Pin description

Pin Number	Symbol	Function	Pin Number	Symbol	Function
1	V_{CC2}	main power supply	5	RST	reset
2	X1	32.768kHz crystal	6	I/O	data input/output
3	X2	32.768kHz crystal	7	SCLK	serial clock input
4	GND	ground	8	V_{CC1}	backup power

Maximum ratings

Parameter	Symbol	Conditions	Rated Value	Unit
Pin-to-ground voltage	V_P		-0.5～+7.0	V
Operating temperature	T_A		0～70	℃
Storage temperature	T_S		-55～+125	℃
Soldering temperature	T_H		260（10 seconds）	℃

Recommended DC operating conditions（T_A=0℃～70℃）

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC1}，V_{CC2}		2.0	5.5	V
logic 1 input voltage	V_{IH}		2.0	V_{CC}+0.3	
logic 0 input voltage	V_{IL}	V_{CC}=2.0V	-0.3	+0.3	V
		V_{CC}=5V	-0.3	+0.8	V

Capacitance（T_A=25℃）

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
input capacitance	C_I			10		pF
I/O capacitance	$C_{I/O}$			15		pF
crystal oscillator capacitance	C_X			6		pF

Electrical properties

DC Characteristics (0℃ to 70℃; V_{CC}＝2.5V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
input current	I_{LI}				500	μA
I/O leakage current	I_{LO}				500	μA
logic 1 output voltage	V_{OH}	V_{CC}=2.5V	1.6			V
		V_{CC}=5V	2.4			
logic 0 output voltage	V_{OL}	V_{CC}=2.5V			0.4	V

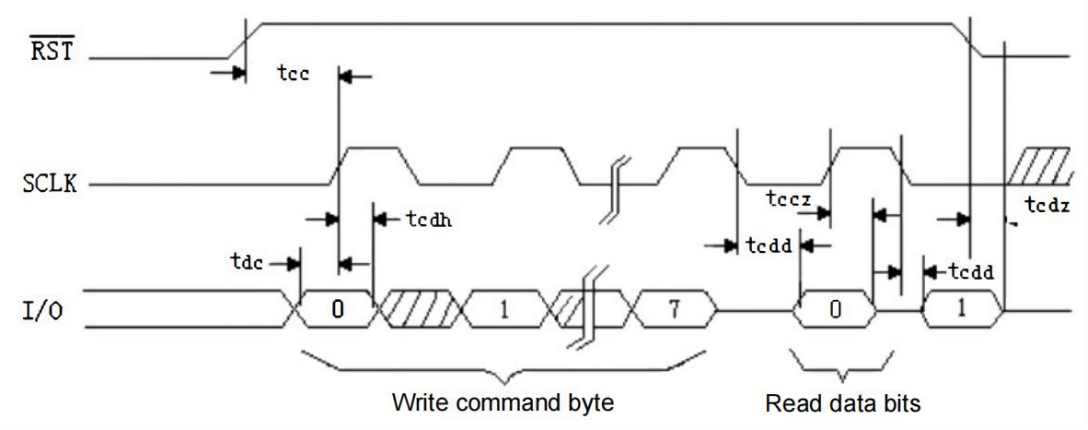
		V_{CC}=5V			0.4	
supply current	I_{CC1A}	V_{CC1}=2.5V			0.4	mA
		V_{CC1}=5V			1.2	
timekeeping current	I_{CC1T}	V_{CC1}=2.5V			0.3	μA
		V_{CC1}=5V			1	
static current	I_{CC1S}	V_{CC1}=2.5V		100		nA
		V_{CC1}=5V		100		
supply current	I_{CC2A}	V_{CC2}=2.5V			0.425	mA
		V_{CC2}=5V			1.28	
timekeeping current	I_{CC2T}	V_{CC2}=2.5V			25.3	μA
		V_{CC2}=5V			81	
static current	I_{CC2S}	V_{CC2}=2.5V			25	μA
		V_{CC2}=5V			80	
trickle charge resistor	R1			2		kΩ
	R2			4		
	R3			8		
trickle charge diode	V_{TD}			0.7		V

AC characteristics (T_A=0℃ to 70℃; V_{CC}=+5V±10%)

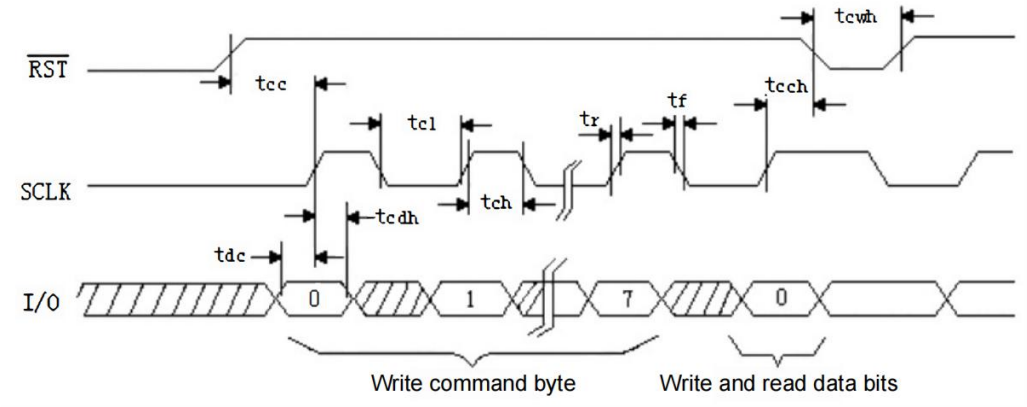
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK to RST hold	t_{cch}	V_{CC}=2.5V	240			ns
		V_{CC}=5V	60			

RST invalid	t_{cwh}	V_{CC}=2.5V	4			ns
		V_{CC}=5V	1			
RST to I/O high-impedance	t_{cdz}	V_{CC}=2.5V			280	ns
		V_{CC}=5V			70	
SCLK to I/O high-impedance	t_{ccz}	V_{CC}=2.5V			280	ns
		V_{CC}=5V			70	
Data to CLK setup	t_{dc}	V_{CC}=2.5V	200			ns
		V_{CC}=5V	50			
CLK to Data hold	t_{cdh}	V_{CC}=2.5V	280			ns
		V_{CC}=5V	70			
CLK to Data delay	t_{cdd}	V_{CC}=2.5V			800	ns
		V_{CC}=5V			200	
CLK low	t_{cl}	V_{CC}=2.5V	1000			ns
		V_{CC}=5V	250			
CLK high	t_{ch}	V_{CC}=2.5V	1000			ns
		V_{CC}=5V	250			
CLK frequency	t_{clk}	V_{CC}=2.5V			0.5	MHz
		V_{CC}=5V	DC		2.0	
CLK rise and fall times	t_r, t_f	V_{CC}=2.5V			2000	ns
		V_{CC}=5V			500	
RST to CLK setup	t_{CC}	V_{CC}=2.5V	4			μs
		V_{CC}=5V	1			

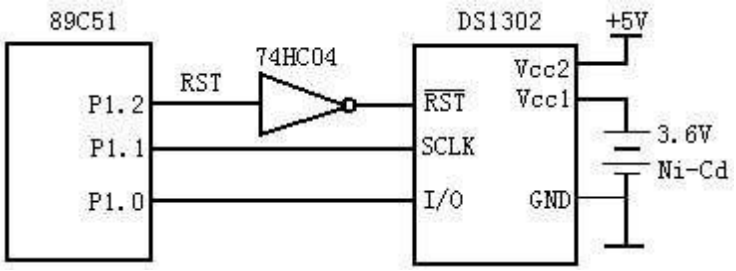
Timing diagram: Read data



Timing diagram: Writing data



Typical application circuit diagram



Instructions for use:

The main components of the serial clock chip are shown in Figure 1: shift register control logic, oscillator, real-time clock, and RAM.

Operation principle: As shown in the diagram, upon the activation of the $\overline{\text{RST}}$ signal, the shift register units serially receive 8-bit instruction bytes from I/O under the control of synchronous SCLK pulse signals. Subsequently, the 8-bit instruction bytes are serialized and transferred to the ROM instruction decoding unit. The ROM instruction decoding unit decodes the 8-bit instruction bytes to determine the addresses of internal registers and their read/write statuses. Following this, under the control of subsequent synchronous SCLK pulse signals, 8-bit data is written into or read from the corresponding registers. Data transfer can also occur in multi-byte mode, where 8-bit instruction bytes are first written, followed by continuous writing or reading of data bytes into/from calendar/clock registers (or RAM units) under consecutive SCLK pulse signals. The number of SCLK pulses is 8 plus 8 in single-byte mode and 8 plus up to 248 in multi-byte mode.

1. Command byte

Command byte details are shown in Figure 2: Each data transfer is initiated by a command byte, where the most significant bit (MSB, bit 7) must be logic 1 for the command to be valid. If it is zero, writing to the DS1302 is disabled. Bit 6, when logic 0, specifies clock/calendar data; when logic 1, it specifies RAM data. Bits 1 to 5 specify particular registers for input or output operations. The least significant bit (LSB, bit 0) is logic 0 for write operations (input) and logic 1 for read operations (output). Command bytes are always input starting from the LSB (bit 0).

1	RAM/CLK	A4	A3	A2	A1	A0	Read/Write

Fig.2 Address/Command Byte

2. Reset and clock control

To initiate all data transfers, drive the RST input to a high logic level. The RST input serves two functions. Firstly, it enables control logic to allow address command sequences to enter the shift register. Secondly, RST can halt data transmission. During data input, data must be valid on the rising edge of the clock, and data bits are output on the falling edge of the clock. If the RST input is at a low logic level, all data transfers cease, and the I/O pin becomes high impedance. Data transfer is illustrated in Figure 3. Upon power-up, RST must be at logic 0 until V_{CC} reaches or exceeds 2.5V; additionally, when driving RST to a logic 1 state, SCLK must be at logic 0.

3. Data input

Following the input of the write command byte, input data on the rising edge of the next 8 SCLK cycles. Any additional SCLK cycles will be disregarded. Input begins with bit 0.

4. Data output

Following the input of the read command byte, output the data byte on the falling edge of the subsequent 8 SCLK cycles. Each data bit being transmitted occurs on the first falling edge after the last bit of the read command byte. As long as RST remains high, any additional SCLK cycles will retransmit the data byte. This operation enables continuous multi-byte read capability. Additionally, on each rising edge of SCLK, the I/O pin enters a high-impedance state. Data output begins with bit 0.

5. Multi-byte mode

By addressing 31-bit addresses (decimal) with address/command bits set to logic 1 from 1 to 5, clock/calendar or RAM registers can be configured for multi-byte mode. As described, bit 6 specifies clock or RAM, and bit 0 specifies read or write. Addresses 9 to 31 in clock/calendar registers or address 31 in RAM registers cannot store data. In multi-byte mode, reading or writing starts from bit 0 of address 0. When writing in multi-byte mode to clock registers, the first 8 registers must be written sequentially as the data is transmitted. However, when writing in multi-byte mode to RAM, it's not necessary to write all 31 bytes. Regardless of whether all 31 bytes are written, each byte written will be transferred to RAM.

Function	Number of bytes	Pulse number
CLOCK	8	72
RAM	31	256

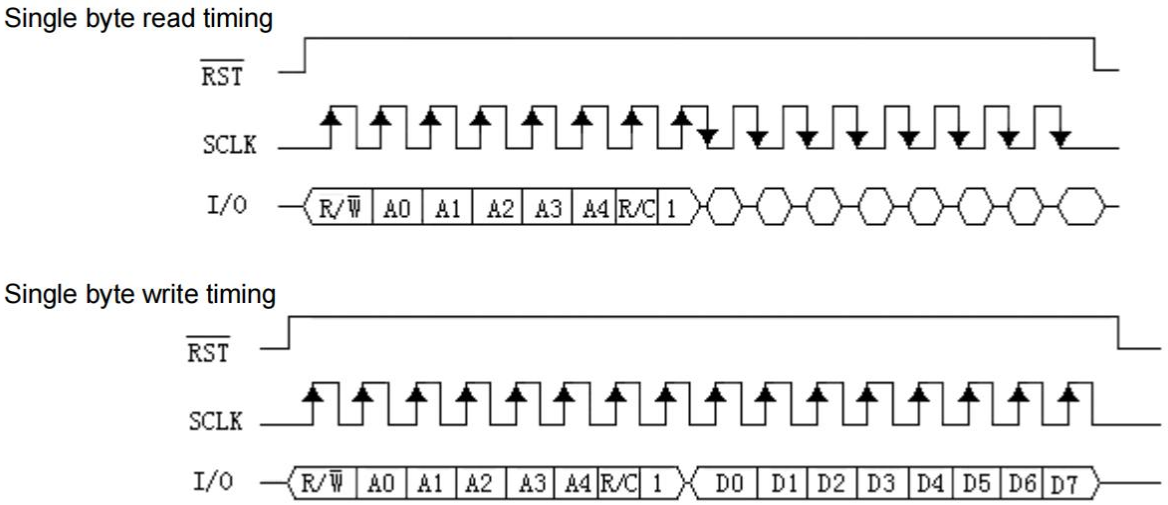


Fig.3 Data Transmission Overview

6. Clock/Calendar

The clock/calendar is contained in seven write/read registers as shown in Figure 4. The data contained in the clock/calendar registers is in binary decimal (BCD) code.

7. Clock pause

Bit 7 of the seconds register is defined as the clock halt bit. When set to logic 1, the clock oscillator stops, putting the DS1302 into a low-power backup mode with power consumption less than 100 nanoamps. Writing this bit to logic 0 starts the clock operation.

8. AM-PM/12-24 mode

Bit 7 of the hour register is defined as the 12/24-hour mode select bit. When set to a high level, it selects the 12-hour mode. In 12-hour mode, bit 5 serves as the AM/PM indicator, with logic high indicating PM. In 24-hour mode, bit 5 represents the second 10-hour bit (20-23 hours).

9. Write protection register

Bit 7 of the write protection register serves as the write protect bit. Initially, the first seven bits (bits 0-6) are set to zero and read as zero during read operations. Before performing any write operation on the clock or RAM, bit 7 must be zero. When set to a high level, the write protect bit prevents writing to any other registers.

10. Trickle charge register

This register governs the DS1302's slow charge characteristics. Figure 4's simplified circuit illustrates the basic components of the slow charger. The slow charge select (TCS) bits (bits 4-7) determine the activation of the slow charger. To prevent accidental activation, only the 1010 mode can engage the slow charger,all other modes disable the slow charger. Upon power-up of the DS1302, the slow charger is disabled. The diode select (DS) bits (bits 2-3) determine whether one or two diodes are connected between V_{CC2} and V_{CC1}. Setting DS to 01 selects one diode, while DS set to 10 selects two diodes.

DS values of 00 or 11 disable the charger, independent of TCS. The resistor select (RS) bits (bits 0-1) determine the resistor connected between V_{CC2} and V_{CC1}. The resistor options for RS selection are as follows:

RS bit	Resistor	Typical Value
00	none	none
01	R1	2kΩ
10	R2	4kΩ
11	R3	8kΩ

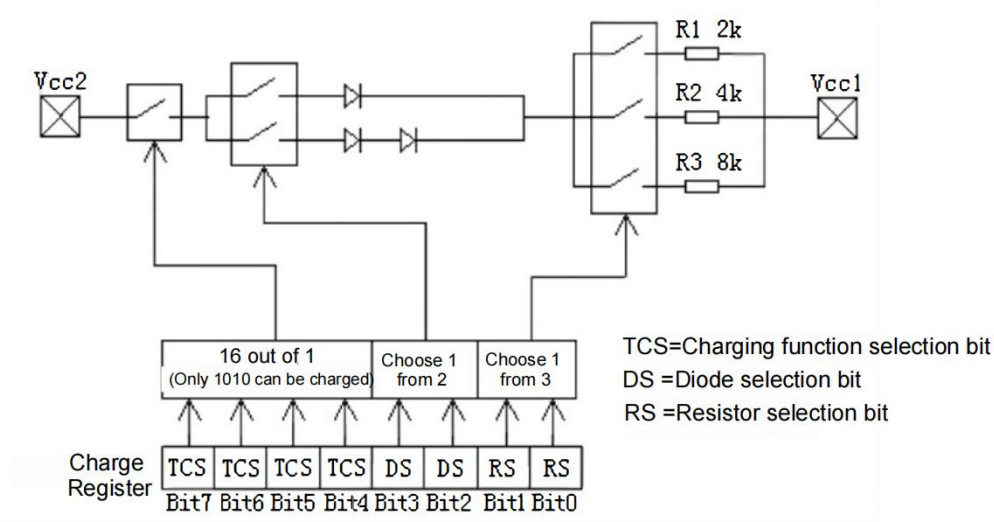


Fig.4 DS1302 Programmable Slow Charger

If RS is 00, the charger is disabled and has nothing to do with TCS.

The selection of diodes and resistors is determined by the maximum current required for charging batteries and supercapacitors. The maximum charging current can be calculated as follows: assuming a 5V system power supply connected to V_{CC2} and a supercapacitor connected to V_{CC1}. Assuming further that during operation of the slow charger, there is a diode and resistor R1 connected between V_{CC2} and $V_{CC}1$. Therefore, the maximum current can be calculated as described below:

$$I_{max} = (5.0V - \text{Diode voltage drop})/R1$$

$$= (5.0V - 0.7V)/2k\Omega$$

$$= 2.2mA$$

It is evident that as the supercapacitor charges, the voltage between V_{CC2} and V_{CC1} decreases, resulting in a reduction of charging current.

11. Clock/calendar multi-byte (Burst) mode

The clock/calendar command byte can specify multi-byte operation mode. In this mode, the first 8 clock/calendar registers can be read or written consecutively starting from bit 0 at address 0 (see Figure 4).

When writing to the clock/calendar in multi-byte mode, if the write-protect bit is set high, no data will be transferred to any of the 8 clock/calendar registers (including the control register). In multi-byte mode, access is not available during slow charging.

12、RAM

The static RAM is a 31×8 byte sequentially addressed space within the RAM address space.

13. RAM multi-byte mode

The RAM command byte can specify multi-byte operation mode. In this mode, it is possible to sequentially read or write 31 bytes of RAM registers starting from bit 0 at address 0 (see Figure 5).

14. Register overview

The register data format is summarized in Figure 5.

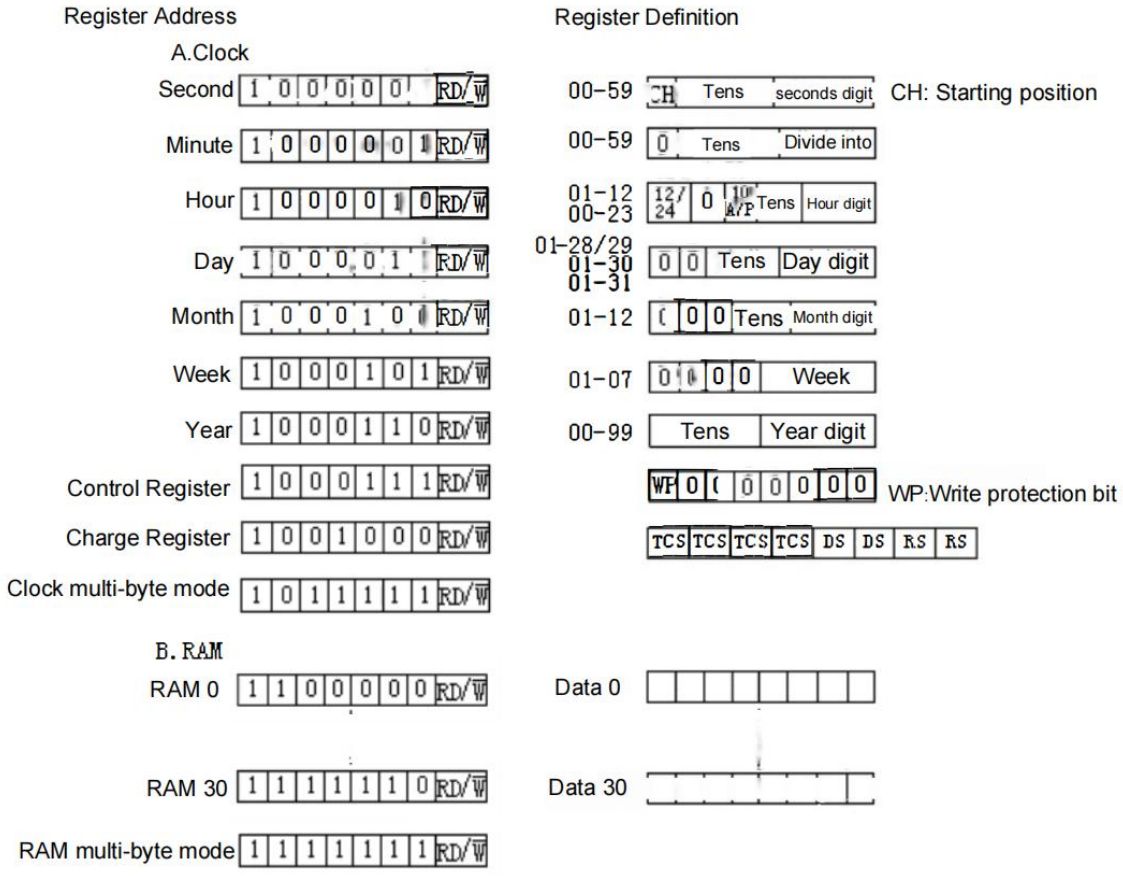


Fig.5 Register Address/Definitio

15. Crystal oscillator selection

A 32.768kHz crystal oscillator can be directly connected to the DS1302 via pins 2 and 3 (X1 and X2). The specified load capacitance (CL) for the chosen crystal should be 6pF.

16. Power Control

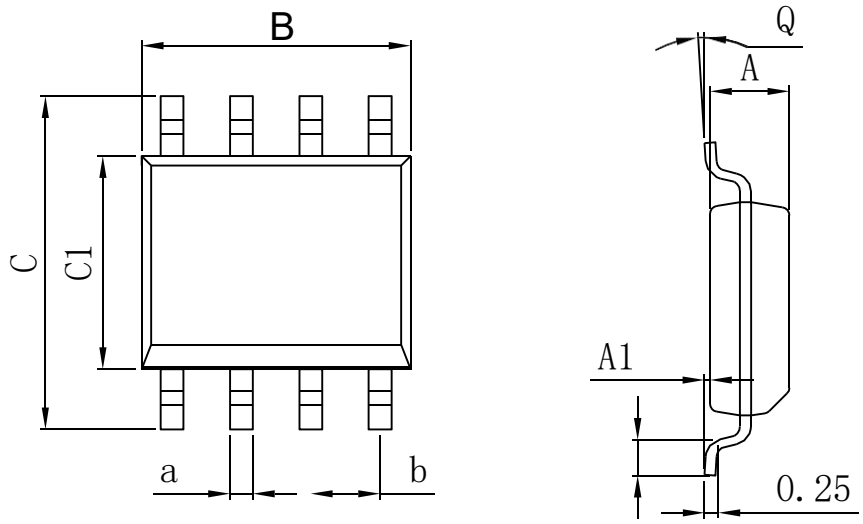
In a system powered by a single source and a battery backup, V_{CC1} provides the low-power battery backup.

In a dual-source system, V_{CC2} serves as the main power source, with V_{CC1} connected to backup power to maintain time and data in the absence of the main power source.

The DS1302 is powered by the higher of VCC1 or V_{CC2}. Specifically, it is powered by V_{CC2} when V_{CC2} is greater than V_{CC1} by at least 0.2V. Conversely, when V_{CC1} is greater than V_{CC2} by at least 0.2V, the DS1302 is powered by V_{CC1}.

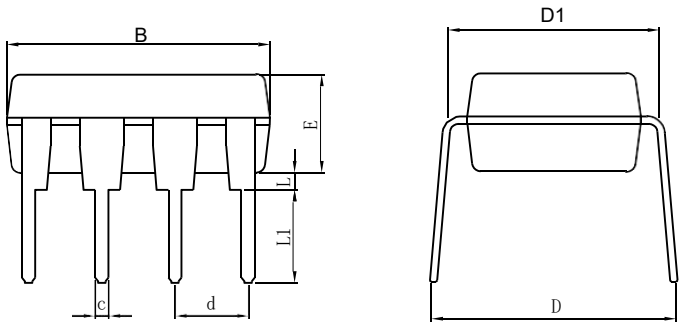
Package dimensions

SOP8



Dimensions In Millimeters					
Symbol:	**Min:**	**Max:**	**Symbol:**	**Min:**	**Max:**
A	1.225	1.570	**D**	0.400	0.950
A1	0.100	0.250	**Q**	0°	8°
B	4.800	5.100	**a**	0.420 TYP	
C	5.800	6.250	**b**	1.270 TYP	
C1	3.800	4.000			

DIP8



Dimensions In Millimeters					
Symbol:	**Min:**	**Max:**	**Symbol:**	**Min:**	**Max:**
A	6.100	6.680	**L1**	3.000	3.600
B	9.000	9.500	**a**	1.524 TYP	
D	8.400	9.000	**b**	0.889 TYP	
D1	7.420	7.820	**c**	0.457 TYP	
E	3.100	3.550	**d**	2.540 TYP	
L	0.500	0.700			