300mA LOW POWER LDO

Overview

SL73xx is a low drop-out linear voltage regulator with the CMOS technology. The maximum output current is 300mA, and the allowed maximum input withstanding voltage is +48V. The device has several fixed output voltage values, with ranges from 1.8V to 5.0V. The COMS technology can ensure the characteristics of low drop-out and low quiescent current.

Functional characteristics and application fields

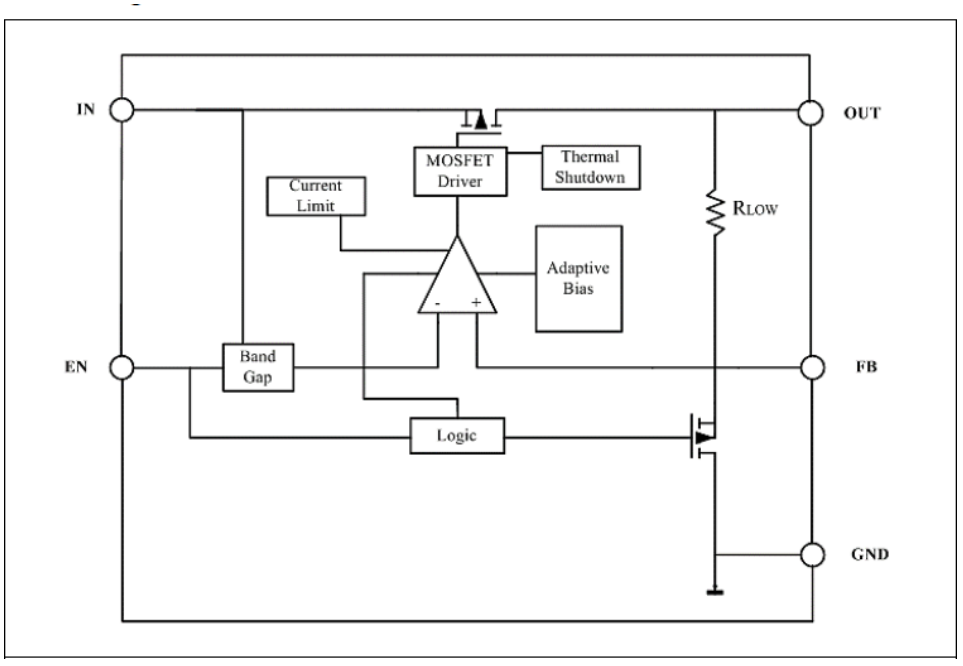
- ★ Low power consumption
- ★ low dropout
- ★ Relatively low temperature coefficient
- ★ Maximum input withstanding voltage: +48V
- ★ Typical quiescent current: 3uA
- ★ Maximum output current: 300mA
- ★ Output voltage accuracy: ±2%
- ★ Package type: SOT23-3, SOT89
- ★ A device with power supply of batteries
- ★ Communication device
- ★ An audio/video device

Table of model selection

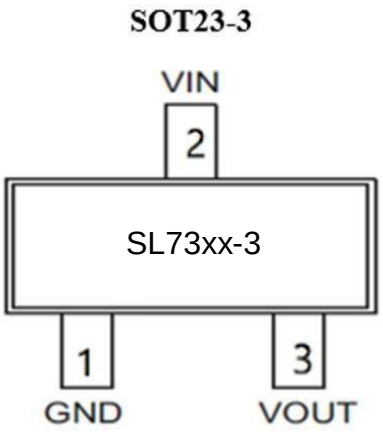
Model	Output voltage	Package type	Positive printing
SL 7318-x	1.8V	SOT23-3 SOT89	73xx-3(packaged as SOT23 -3) 73xx-8(packaged as SOT89 -3)
SL 7325-x	2.5V		
SL 7330-x	3.0V		
SL 7333-x	3.3V		
SL 7336-x	3.6V		
SL 7344-x	4.4V		
SL 7350-x	5.0V		

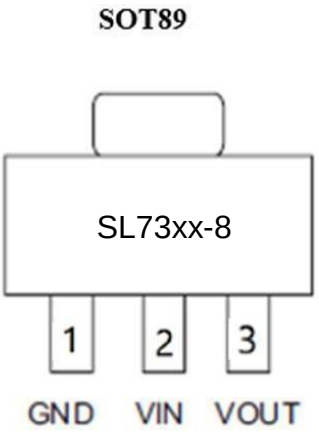
Notes: "xx" represents for the output voltage.

Circuit functional block diagram



Pin drawing





Pin instruction

No. of pins	Name of pins	Description
1	GND	Ground
2	VIN	Power supply input pin
3	VOUT	Output pin, required to be connected to the ground with a capacitor higher than 1uF

Absolute parameters

	Description	Values	Units
Vin	Input voltage	0~+45(Note1)	V
Vout	Output voltage	1.8~5.0	V
Tstg	Storage temperature	-45~+140	℃
TWK	Working temperature	-40~+85	℃
ESD_{HBM}	Human body mode	4000(Note2)	V
CDM	voltage live device mode	1500(Note2)	V
Latch up	Latch maximum rated current value	200(Note2)	mA

Only rated power is emphasized here; working with the power out of the ranges of the absolute parameters will lead to damages to the chip, and it is difficult to expect the working state of the chip out of the ranges marked above; in addition, long-term working out of the marked ranges may lead to influences on reliability of the chip.

Note 1: Refer to electrical characteristics and application information.

Note2： The ESD protection of the series of products has been tested with the following testing methods:

The ESD human body mode is tested according to EIA/JESD22-A114.

The electrostatic discharging ability is tested according to JESD22-C101.

The latch maximum current value is tested according to JEDEC78.

Suggested working conditions

Parameters	Description	Ranges	Units
VIN	Input voltage	+2.5~+45	V
IOUT	Output current	0~300	mA
TA	Working temperature	-40~+85	℃
CIN	Capacitor pol on the input end	1~10	uF
COUT	Capacitor pol on the output end	1~10	uF
ESR	The equivalent resistance value on the input end and the output end	5~100	mΩ

Thermal energy information

Symbols	**Parameters**	**Package type**	**Max. value**	**Units**
θ_{JA}	Thermal resistance (connecting with environment) (assumed with no environment airflow or cooling fin)	SOT23-3	360	℃/W
		SOT89	135	℃/W
P_D	Power consumption	SOT23-3	0.2	W
		SOT89	0.5	W

Notes: The P_D value is measured at Ta=25℃.

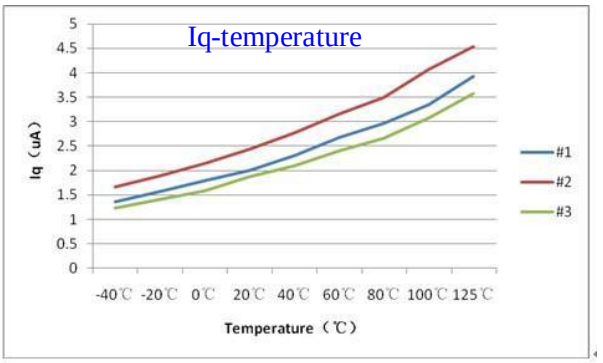
Electrical characteristics

Ta=25℃

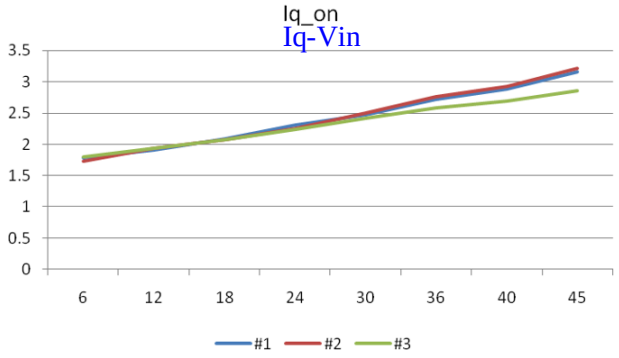
Symbols	Parameters	Testing conditions	Min.	Typical	Max.	Units
VIN	Input voltage	—	—	—	+45	V
V_{OUT}	Output voltage	T_A=+25V℃	-2%		+2%	V
		-40℃≤T_A≤+85℃	-3%		+3%	V
V_{DROP}	Dropout voltage =300mA	V_{OUT} =1.8V	—	1350	1650	mV
		V_{OUT} =2.5V	—	1150	1450	mV
		V_{OUT} =2.8V	—	1100	1400	mV
		V_{OUT} =3.0V	—	1050	1350	mV
		V_{OUT} =3.3V	—	1000	1300	mV
		V_{OUT} =4.4V	—	950	1250	mV
		V_{OUT} =5V	—	900	1200	mV
I_{OUT}	Output current	V_{IN}=V_{OUT}+2V	—	300	—	mA
$Load_{Reg}$	Load regulation ratio	1mA≤V_{OUT}≤300mA V_{IN} =Vout+1V	—	—	40	mV
I_LMT	Limited current	V_{IN}=V_{OUT}+1V	300	450	—	mA
I_{SHORT}	Short circuit limited current	V_{OUT} =0V	—	100	—	mA
I_Q	Quiescent current	No load (=0mA)	—	3	4.0	uA
PSRR	Power supply rejection ratio	V_{IN}=V_{OUT}+1V, I_{OUT}=20mA f=1KHz	—	60	—	dB
eN	Output Noise Voltage	V_{IN}=V_{OUT}+1V, I_{OUT}=1mA f=10Hz~100KH z (V_{OUT}=3V) C_{out} =1uF	—	100	—	uVrms
R_{LOW}	Output discharge resistance	=4V,Ven=0V	—	70	—	Ω
$\frac{\triangle VOUT}{\triangle VIN \times VOUT}$	Input voltage regulation ratio	Vo+1V≤V_{IN}≤45V I_{OUT} =1mA	—	—	0.2	%/V
$\frac{\triangle VOUT}{\triangle Ta \times VOUT}$	Temperature coefficient	I_{OUT} =10mA -40℃<Ta<85℃	—	100	—	ppm/℃

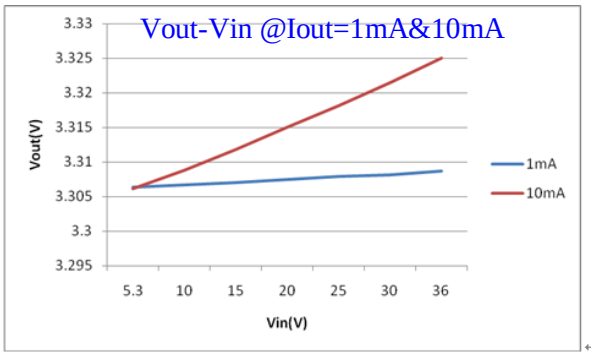
Notes: Make the output voltage drop by 2% in the condition of VIN=VOUT+2V and a fixed load; the difference of the input voltage and the output voltage at this time is the Dropout voltage.

Typical performance characteristics

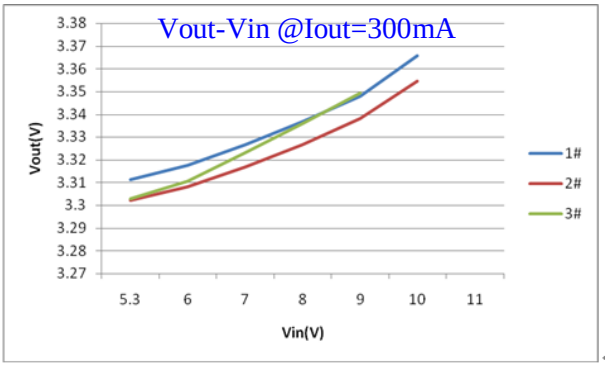


DC Supply Quiescent Current

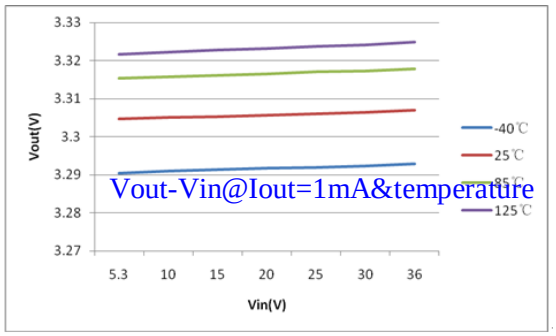




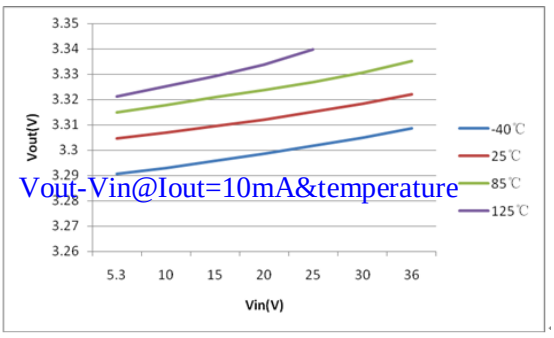
Line Regulation



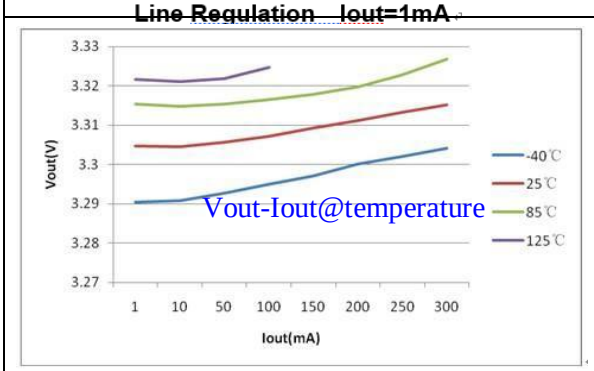
Iout=300mA Line Regulation



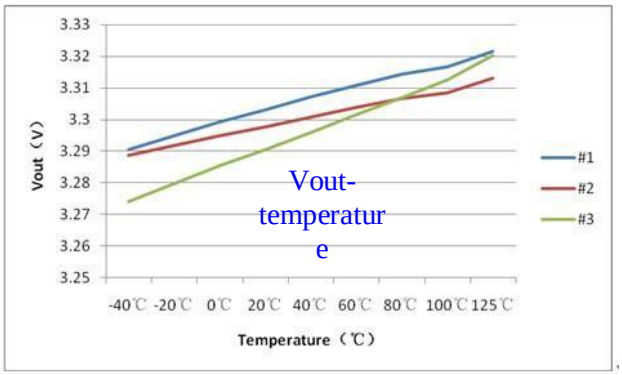
Line Regulation Iout=1mA



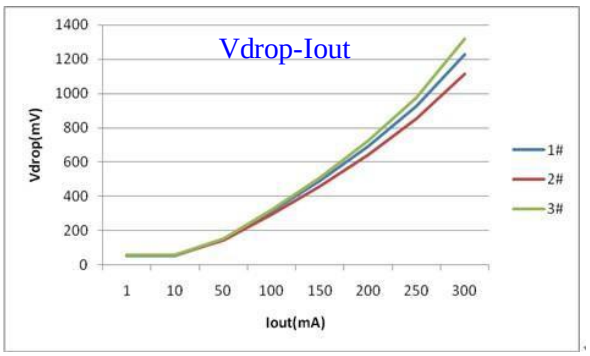
Line Regulation Iout=10mA

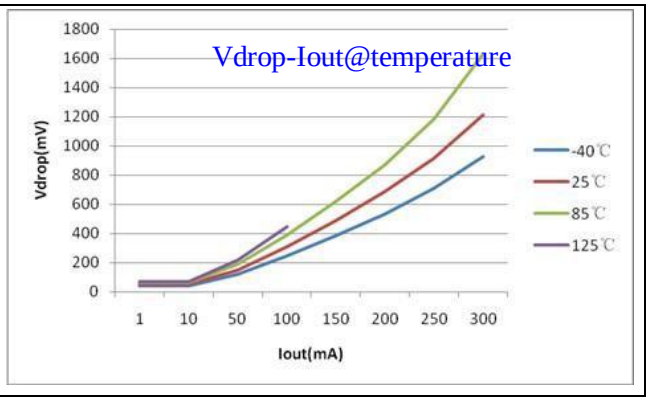


Load Regulation

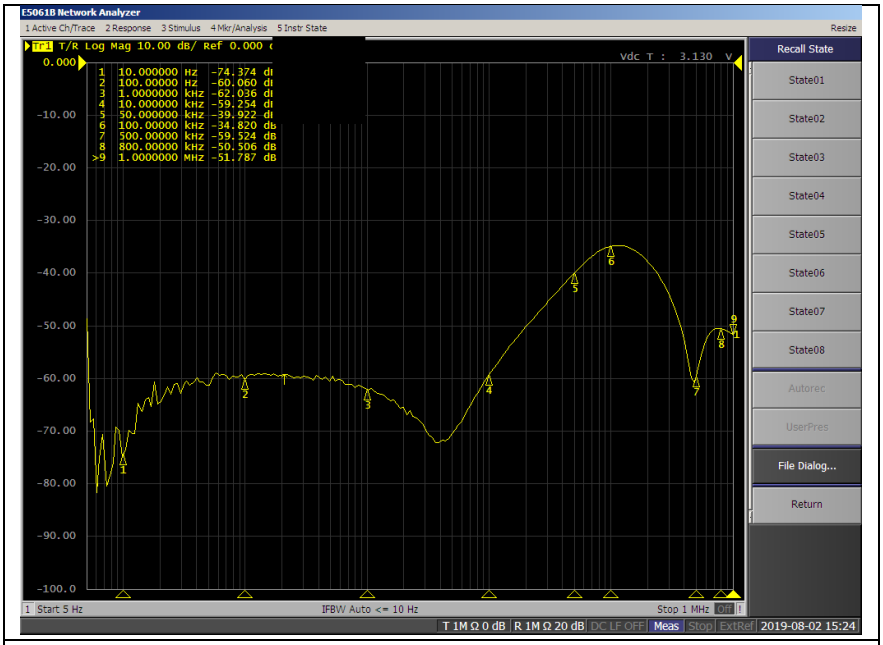


Output Voltage

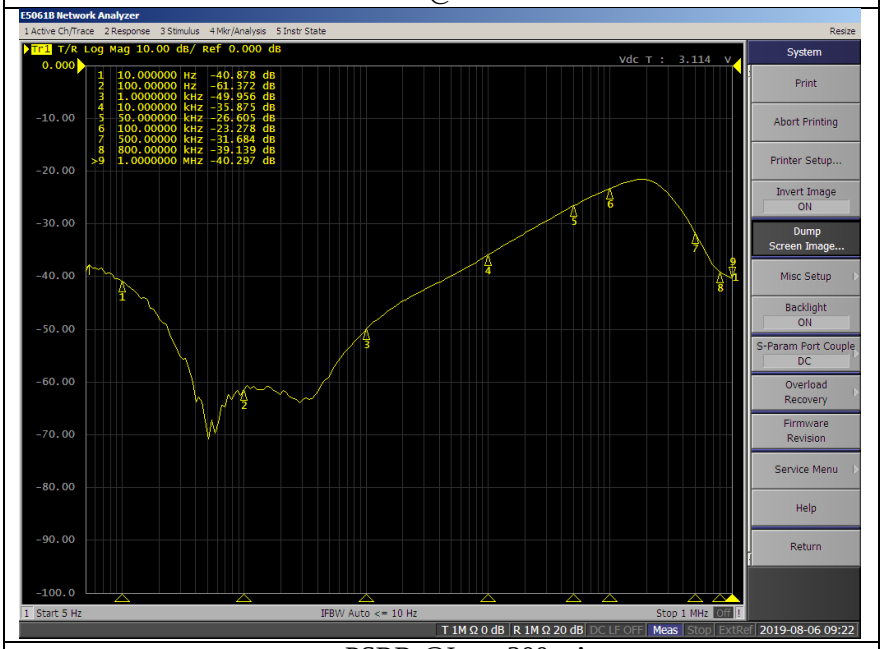




PSSR:



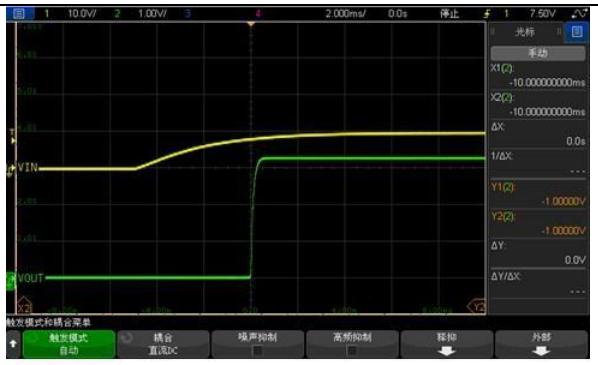
PSRR @Iout=20mA



PSRR @Iout=300mA

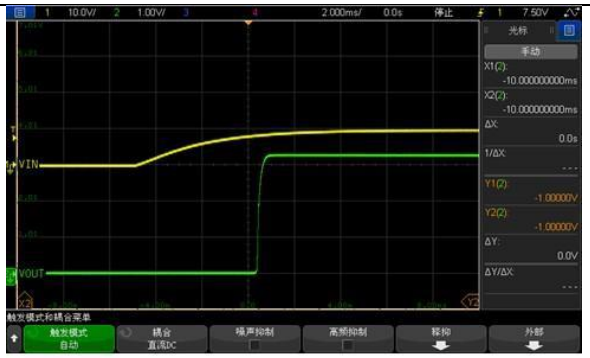
Starting characteristic:

Vin=10V, Iout=0mA,Cout=0.1uF



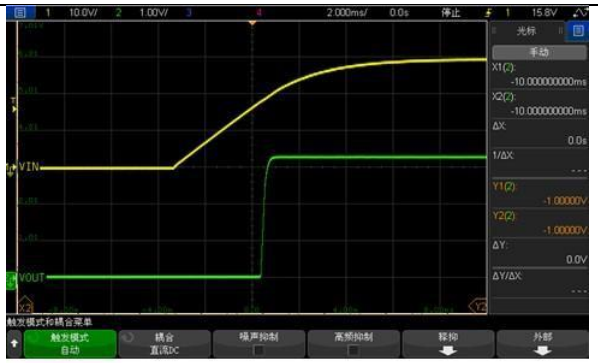
Vin=10V, Iout=0mA,Cout=10uF

Vin=10V, Iout=30mA,Cout=0.1uF

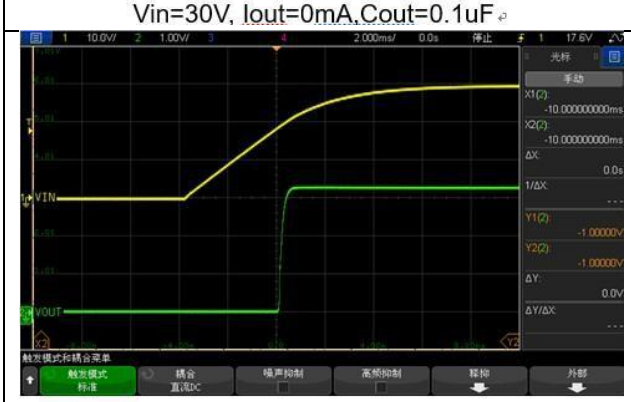


Vin=10V, Iout=30mA,Cout=10uF

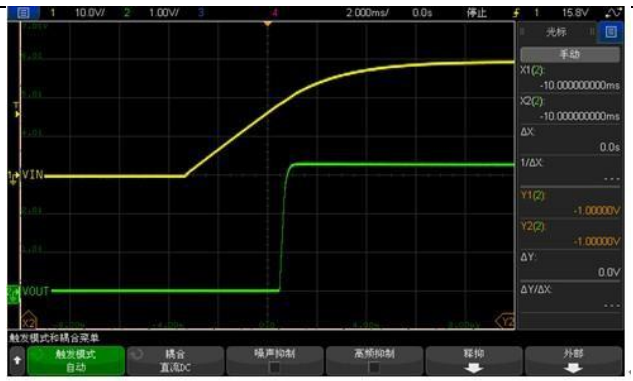
Vin=30V, Iout=0mA,Cout=0.1uF



Vin=30V, Iout=0mA,Cout=10uF



Vin=30V, Iout=30mA,Cout=0.1uF



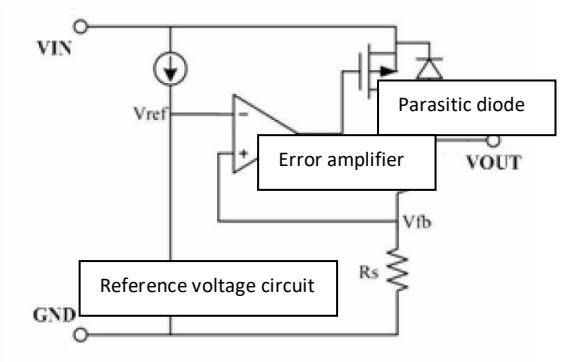
Vin=30V, Iout=30mA,Cout=10uF

Current-limiting protection

With the current-limiting protection function, it can prevent the device from damages in condition of overloading or short circuit. The current is tested by the internal induction transistor.

Functional description

The error amplifier compares the input voltage Vfb, which is the divider resistance composed by the feedback resistance Rs and Rf, with the reference voltage Vref. Provide necessary gate pole voltage to the output transistor through the error amplifier, to prevent the output voltage from influences of the input voltage or the temperature, to kept it unchanged.



Matters needing attention:

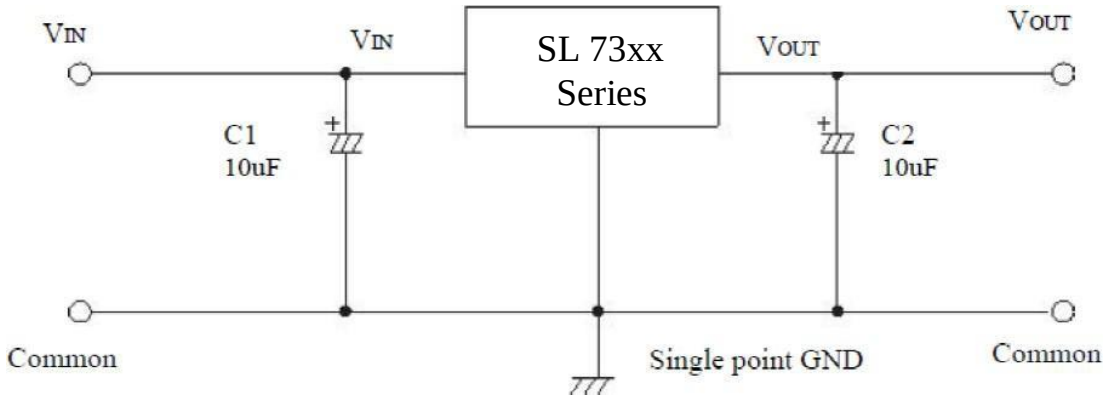
1) The phase compensation and the ESR of the output capacitor are utilized in the circuit for compensation; therefore, it is suggested to connect a capacitor larger than 1uF between the output and the ground.
2) It is suggested to use a polar capacitor of 10uF for the input and the output, and try to make the capacitor get closer to the pins of VIN and VOUT of LDO.
3) Pay attention to using conditions of the input and output voltage and the loading current, to prevent the condition that the internal power consumption (PD) of IC exceeds the allowed maximum power consumption by package.

   The calculation method of PD: PD=(VIN－VOUT)×IOUT

   For example: SL 7350-8, SOT89 package, when VIN=12V, IOUT=100mA, PD=（12-5）×100mA=0.7W，

   It may lead to damage to IC if it exceeds 0.5W than the specified value. With respect to the PD value of different package modes, please refer to the column of "thermal energy information".

Typical application circuit

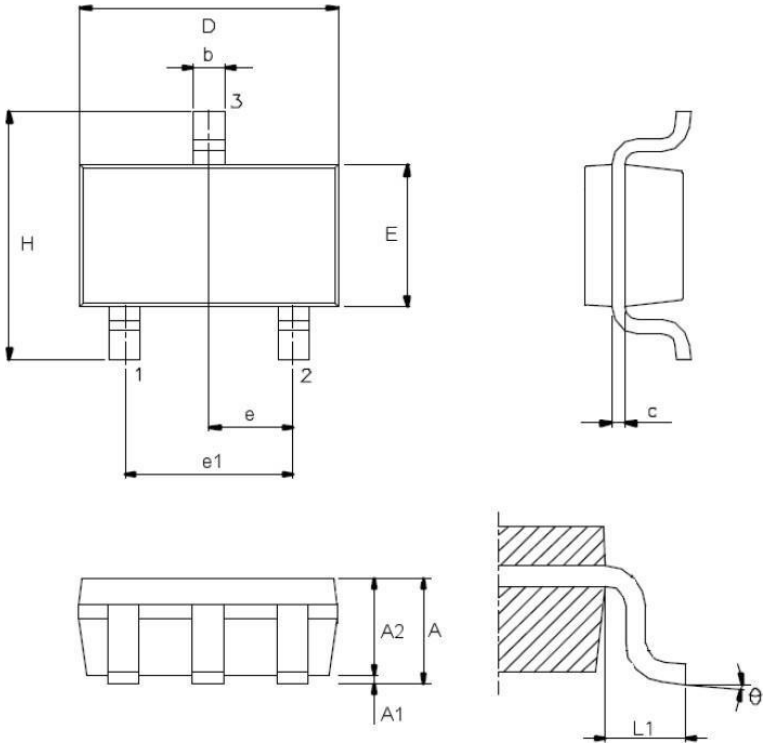


Layout suggestions:

1. Try to make the input and the output capacitor get closer to the device.
2. Conduct device connection with a copper plane, to optimize the thermal performance.
3. Arrange simulated thermal vias around the device, to make thermal energy dispersed.

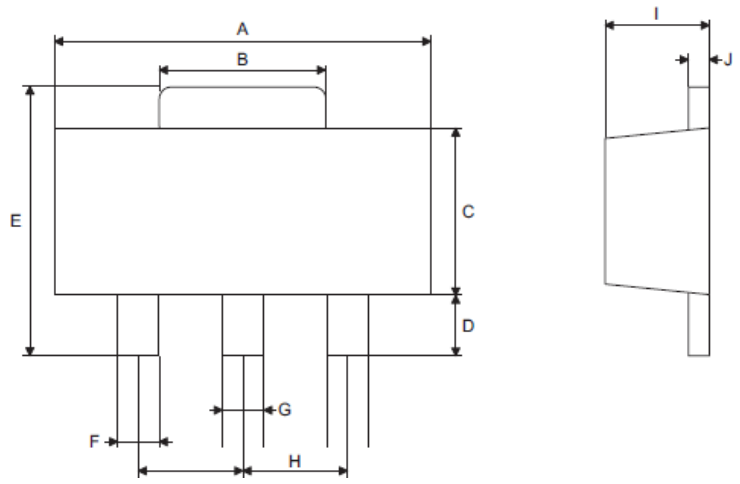
Package information

SOT23-3 package dimension



Symbols	Dimension (nits: mm)		
	Min.	Typical	Max.
A	—	—	1.45
A1	—	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
C	0.08	—	0.22
D	—	2.90	—
E	—	1.60	—
e	—	0.95	—
e1	—	1.90	—
H	—	2.80	—
L1	—	0.60	
θ	0°	—	9°

SOT89 package dimension



Symbols	Dimension (nits: mm)		
	Min.	Typical	Max.
A	4.40	—	4.60
B	1.35	—	1.83
C	2.29	—	2.60
D	0.89	—	1.20
E	3.94	—	4.25
F	0.36	—	0.48
G	0.44	—	0.56
H	—	1.50	—
I	1.40	—	1.60
J	0.35	—	0.44