500mA Ultra-Low Noise Ultra-Fast Response LDO Linear Regulator

Description

The SL703xx series is a CMOS buck voltage regulator with high ripple rejection, low power consumption, and low dropout voltage, featuring overcurrent and short-circuit protection. These devices exhibit a very low quiescent current (40A Typ.) and can provide 300mA of output current with a minimal input-to-output voltage differential while maintaining good regulation. Due to their minimal voltage drop and low quiescent current, these devices are especially suitable for battery-powered products that aim to extend useful battery life, such as computers, consumer electronics, and industrial equipment.

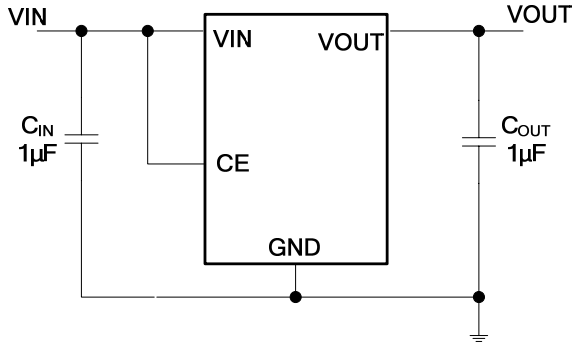
Features

- Output range：1.0V-5.0V
- 500mA output current
- High power rejection ratio: 70 dB 1 kHz
- Very low quiescent bias current: 40ua (typical)
- Less than 1μA in shutdown mode
- Temperature operation at the junction from -40 °C to +85 °C

Applications

- CDMA / GSM cell
- phones
- PDAs/MP3
- WLAN and Bluetooth devices
- cordless telephone
- Battery powered systems

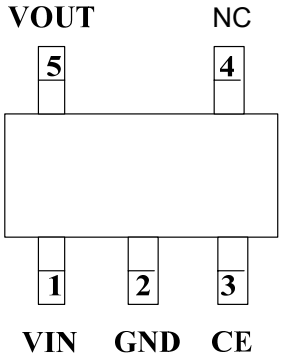
Typical Application



The pins in the figure are schematic and not physical pins

Pinout

SOT23-5



The foot position is determined by the direc tion of the marking text

Package Dissipation Rating

Package	Pd(mW)
SOT23-5	300

Limit parameters

Parameters	Symbol	Limit value	Unit
Vin Pin Voltage	V_{IN}	6	V
Vout Leg Current	I_{out}	300	mA
Vout Pin Voltage	V_{out}	Vss-0.3 ~ Vout+0.3	V
Operating temperature	T_{Opr}	-40 ~ +85	℃
storage temperature	T_{stg}	-55 ~ +125	℃
Welding temperature and time	T_{solder}	260℃, 10s	℃

note: Exceeding the Absolute Limit Parameters may destroy the device. Devices will operate within the recommended operating range, but their characteristics are not guaranteed.
Prolonged operation at the absolute limit parameters may affect the reliability of the device.

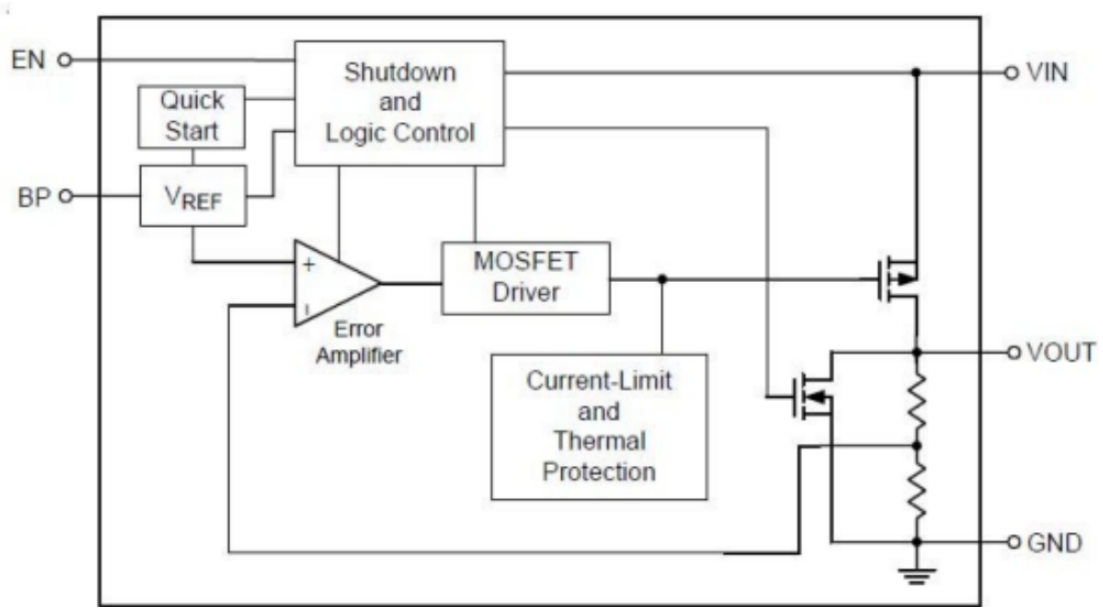
Pin Description

Pin number	Pin name	I/O	Descriptive
1	VIN	P	power supply side
2	GND	O	grounding terminal
3	CE	I	i.e. EN, enable terminal
4	NC	N	unoccupied
5	VOUT	I	output side

Model Selection

Name	Model number	Maximum input voltage (V)	Output voltage (V)	Package form
	SL703xx	7.0	1.2，1.5，1.8，2.5，2.8，3.0，3.3，5.0	SOT23-5
Description of model selection: the first XX output voltage value; such as: SL70312 is 1.2V output voltage.				

Structural block diagram



Main parameters and working characteristics

(Vin=Vout+1V,Cin=Cout=1u,Ta=25℃. Unless otherwise specified)

Characterization	Symbol	Test conditions	Min	Typ	Max	Unit
Output voltages	V_{OUT}(E) (Note 2)	I_{OUT}=40mA, V_{IN}=Vout+1V	X 0.98	V_{OUT} (T) (Note 1)	X 1.02	V
Input voltage	V_{IN}				7.0	V
Maximum output current	I_{OUT}max	V_{IN}=Vout+1V	300			mA
Load charact eristics	ΔV_{OUT}	V_{IN}=Vout+1V, 1mA≤I_{OUT}≤100mA		50		mV
Differential pressure (Note 3)	V_{dif1}	I_{OUT} =100mA		300		mV
	V_{dif2}	I_{OUT} =200mA		500		mV
Quiescent current	I_{SS}	V_{IN}=Vout+1V		40		μA
Shutdown current	I_{CEL}	Vce＝0V		1		μA
Supply voltage adjustment ratio	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \bullet V_{OUT}}$	I_{OUT} =40mA Vout+1V ≤V_{IN}≤8V		0.05		%/V
Output noise	en	I_{OUT} =40mA, 300Hz~50kHz		50		uVrms
Ripple rejection ratio	PSRR	Vin= [Vout+1]V +1Vp-pAC I_{OUT} =40mA,f=1kHz		70		dB

Note: 1, V_{OUT} (T): the specified output voltage

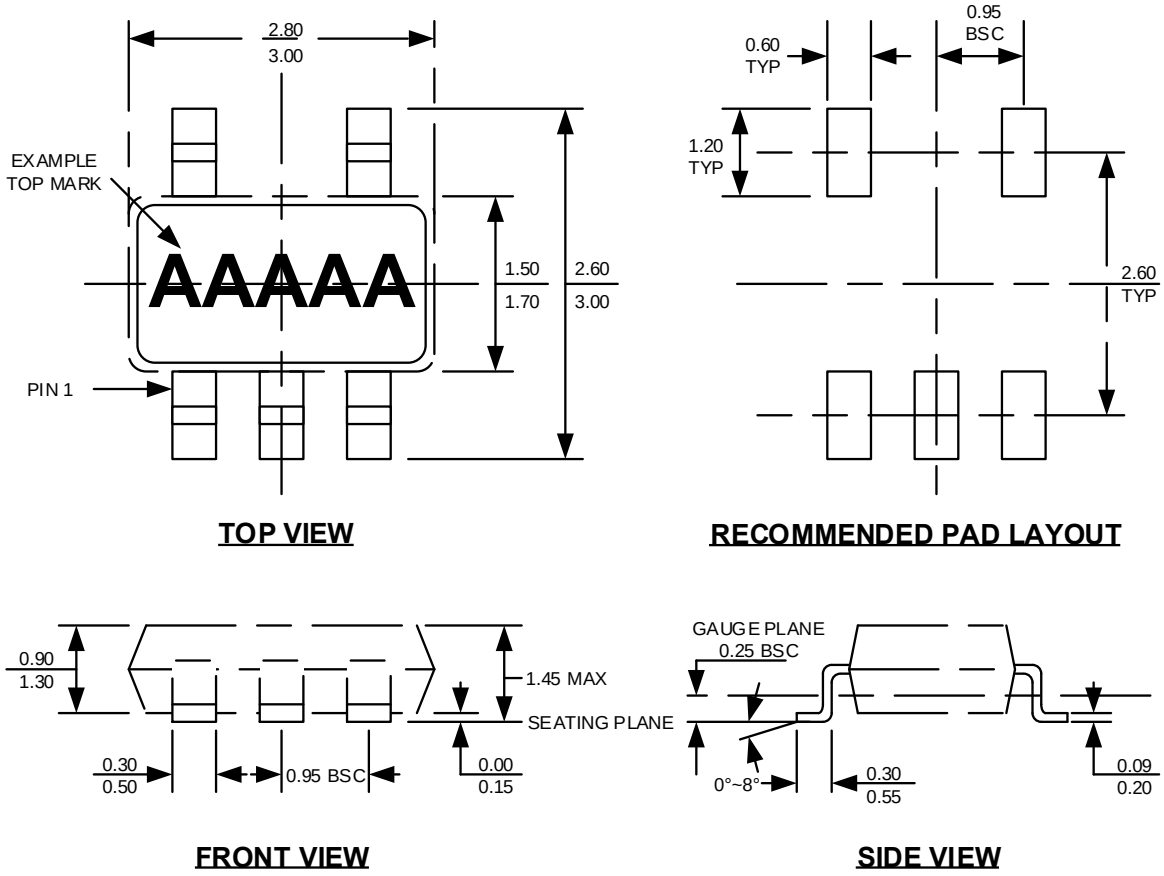
2、 V_{OUT} (E) : Effective output voltage (i.e., when I_{OUT} maintains a certain value, V_{IN} = (V_{OUT} (T) + 1.0V) when the output voltage.

3、 Vdif ：V_{IN}1 -V_{OUT} (E)'

V_{IN}1 : Gradually reduce the input voltage, when the output voltage drops to 98% of V_{OUT} (E), V_{OUT} (E)' = V_{OUT} (E) X 98%

Package Size

SOT23-5



TOP VIEW **RECOMMENDED PAD LAYOUT**

FRONT VIEW **SIDE VIEW**